Voltage Controlled Oscillator

This volume includes extended and revised versions of a set of selected papers from the 2011 2nd International Conference on Education and Educational Technology (EET 2011) held in Chengdu, China, October 1-2, 2011. The mission of EET 2011 Volume 2 is to provide a forum for researchers, educators, engineers, and government officials involved in the general areas of education management, education theory and education application to disseminate their latest research results and exchange views on the future research directions of these fields. 133 related topic papers were selected into this volume. All the papers were reviewed by 2 program committee members and selected by the volume editor Prof. Yuanzhi Wang, from Intelligent Information Technology Application Research Association, Hong Kong. The conference will bring together leading researchers, engineers and scientists in the domain of interest. We hope every participant can have a good opportunity to exchange their research ideas and results and to discuss the state of the art in the areas of the education management, education theory and education application.

Design of High-Performance CMOS Voltage-Controlled Oscillators presents a phase noise modeling framework for CMOS ring oscillators. The analysis considers both linear and nonlinear operation. It indicates that fast rail-to-rail switching has to be achieved to minimize phase noise. Additionally, in conventional design the flicker noise in the bias circuit can potentially dominate the phase noise at low offset frequencies. Therefore, for narrow bandwidth PLLs, noise up conversion for the bias circuits should be minimized. We define the effective Q factor (Qeff) for ring oscillators and predict its increase for CMOS processes with smaller feature sizes. Our phase noise analysis is validated via simulation and measurement results. The digital switching noise coupled through the power supply and substrate is usually the dominant source of clock jitter. Improving the supply and substrate noise immunity of a PLL is a challenging job in hostile environments such as a microprocessor chip where millions of digital gates are present.

The increasing demand for extremely high-data-rate communications has urged researchers to develop new communication systems. Currently, wireless transmission with more than one Giga-bits-per-second (Gbps) data rates is becoming essential due to increased connectivity between different portable and smart devices. To realize Gbps data rates, millimeter-wave (MMW) bands around 60 GHz is attractive due to the availability of large bandwidth of 9 GHz. Recent research work in the Gbps data rates around 60 GHz band has focused on short-range indoor applications, such as uncompressed video transfer, high-speed file transfer between electronic devices, and communication to and from kiosk. Many of these applications are limited to 10 m or less, because of the huge free space path loss and oxygen absorption for 60 GHz band MMW signal. This book introduces new knowledge and novel circuit techniques to design

low-power MMW circuits and systems. It also focuses on unlocking the potential applications of the 60 GHz band for high-speed outdoor applications. The innovative design application significantly improves and enables high-data-rate low-cost communication links between two access points seamlessly. The 60 GHz transceiver system-on-chip provides an alternative solution to upgrade existing networks without introducing any building renovation or external network laying works.

The book discusses the latest developments and outlines future trends in the fields of microelectronics, electromagnetics and telecommunication. It contains original research works presented at the International Conference on Microelectronics, Electromagnetics and Telecommunication (ICMEET 2018), organised by GVP College of Engineering (A), Andhra Pradesh, India. The respective papers were written by scientists, research scholars and practitioners from leading universities, engineering colleges and R&D institutes from all over the world, and share the latest breakthroughs in and promising solutions to the most important issues facing today’s society.

Design of Monolithic Emitter Degenerated Voltage-controlled Oscillators

A voltage-controlled oscillator using the 90 nm CMOS technology has been presented with the total power dissipation of 14 mW, which provides 1.7 mW of total output power. It has highly linear voltage to frequency transformation, with only 4.85% of maximum error. This VCO works in the long range from 5.1 to 9.099 GHz. The controlling voltage varies from 0 to 0.5 volts. The oscillator is powered by a 1 volt power supply.

Two kinds of voltage-controlled oscillators (VCO)--active inductor based VCO and LC cross-coupled VCO--are studied in this work. Although the phase noise performance is not competitive, the proposed active inductor based VCO provide an alternative method to VCO design with very small chip area and large tuning range. The measurement shows a test oscillator based on active inductor topology successfully oscillates near 530MHz band. The phase noise of the widely used LC cross-coupled VCO is extensively investigated in this work. Under the widely used power dissipation and chip area constraints, a novel optimization procedure in LC oscillator design centered on a new inductance selection criterion is proposed. This optimization procedure is based on a physical phase noise model. From it, several closed-form expressions are derived to describe the phase noise generated in the LC oscillators, which indicate that the phase noise is proportional to the L2· gL3 factor. The minimum value of this factor for an area-limited spiral inductor is proven to monotonically decrease with increasing inductance, suggesting a larger inductance is helpful to reduce the phase noise in LC VCO design. The validity of the optimization procedure is proven by simulations. Two test chips are designed and measured.

Summarizes the schemes and technologies in RF circuit design, describes the basic parameters of an RF system and the fundamentals of RF system design, and presents an introduction of the individual RF circuit block design. Forming the backbone of today's mobile and satellite communications networks, radio frequency (RF) components and circuits are incorporated into everything that transmits or receives a radio wave, such as mobile phones, radio, WiFi, and walkie talkies. RF Circuit Design, Second Edition immerses practicing and aspiring industry professionals in the complex world of RF design. Completely restructured and reorganized with new content, end-of-chapter exercises, illustrations, and an appendix, the book presents integral information in three complete sections: Part One explains the different

methodologies between RF and digital circuit design and covers voltage and power transportation, impedance matching in narrow-band case and wide-band case, gain of a raw device, measurement, and grounding. It also goes over equipotentiality and current coupling on ground surface, as well as layout and packaging, manufacturability of product design, and radio frequency integrated circuit (RFIC). Part Two includes content on the main parameters and system analysis in RF circuit design, the fundamentals of differential pair and common-mode rejection ratio (CMRR), Balun, and system-on-a-chip (SOC). Part Three covers low-noise amplifier (LNA), power amplifier (PA), voltage-controlled oscillator (VCO), mixers, and tunable filters. RF Circuit Design, Second Edition is an ideal book for engineers and managers who work in RF circuit design and for courses in electrical or electronic engineering.

Today's complex electronic systems with billions of transistors on a single die are enabled by the aggressive scaling down of the device feature size at an exponential rate as predicted by the Moore's law. Digital circuits benefit from technology scaling to become faster, more energy efficient as well as more area efficient as the feature size is scaled down. Moreover, digital design also benefits from mature CAD tools that simplify the design and cross-technology porting of complex systems, leveraging on a cell-based design methodology. On the other hand, the design of analog circuits is getting increasingly difficult as the feature size scales down into the deep nanometer regime due to a variety of reasons like shrinking voltage headroom, reducing intrinsic gain of the devices, increasing noise coupling between circuit nodes due to shorter distances etc. Furthermore, analog circuits are still largely designed with a full custom design ow that makes their design and porting tedious, slow, and expensive. In this context, it is attractive to consider realizing analog/mixed-signal circuits using standard digital components. This leads to scaling-friendly mixed-signal blocks that can be designed and ported using the existing CAD framework available for digital design. The concept is already being applied to mixed-signal components like frequency synthesizers where all-digital architectures are synthesized using standard cells as basic components. This can be extended to other mixed-signal blocks like digital-to-analog and analog to- digital converters as well, where the latter is of particular interest in this thesis. A voltage-controlled oscillator (VCO)-based analog-to-digital converter (ADC) is an attractive architecture to achieve all-digital analog-to digital conversion due to favorable properties like shaping of the quantization error, inherent anti-alias filtering etc. Here a VCO operates as a signal integrator as well as a quantizer. A converter employing a ring oscillator as the VCO lends itself to an all-digital implementation. In this dissertation, we explore the design of VCO-based ADCs synthesized using digital standard cells with the long-term goal of achieving high performance data converters built from low accuracy switch components. In a first step, an ADC is designed using vendor supplied standard cells and fabricated in a 65 nm CMOS process. The converter delivers an 8-bit ENOB over a 25 MHz bandwidth while consuming 3.3 mW of power resulting in an energy efficiency of 235 fJ/step (Walden FoM). Then we utilize standard digital CAD tools to synthesize converter designs that are fully described using a hardware description language. A polynomial-based digital post-processing scheme is proposed to correct for the VCO nonlinearity. In addition, pulse modulation schemes like delta modulation and asynchronous sigma-delta modulation are used as a signal pre-coding scheme, in an attempt to reduce the impact of VCO nonlinearity on converter performance. In order to investigate the scaling benefits of all-digital data conversion, a VCO-based converter is designed in a 28 nm CMOS process. The design delivers a 13.4-bit ENOB over a 5 MHz bandwidth achieving an energy efficiency of 4.3 fJ/step according to post-synthesis schematic simulation, indicating that such converters have the potential of achieving good performance in deeply scaled processes by exploiting scaling benefits. Furthermore, large conversion errors caused by non-ideal sampling of the oscillator phase are studied. An encoding scheme employing ones counters is proposed to code the sampled ring oscillator output into a number, which is resilient to a class of sampling induced errors modeled by temporal reordering of

the transitions in the ring. The proposed encoding reduces the largest error caused by random reordering of up to six subsequent bits in the sampled signal from 31 to 2 LSBs. Finally, the impact of process, voltage, and temperature (PVT) variations on the performance while operating the converter from a subthreshold supply is investigated. PVT-adaptive solutions are suggested as a means to achieve energy-efficient operation over a wide range of PVT conditions.

The voltage-controlled oscillator (VCO) is one of the most important building blocks in data communication systems. The design of high performance monolithic integrated VCO is extremely challenging and is still an active research area. In this dissertation, the emitter degeneration technique is presented. The concept is first explained intuitively, refined later by more accurate models. The benefits of emitter degeneration are analytically proven, and also verified through simulation and experimentation. Design equations, design and layout guidelines are provided. Using SiGe BiCMOS technology, four VCOs and a clock recovery circuits are fabricated as strong evidence of the usefulness of this technique. Comparisons to recent publications are also conducted. The developed capacitive emitter degeneration technique is applicable to future VCOs because it is process independent, and its ability to simultaneously increase oscillation frequency, tuning range while improving phase noise makes it an extremely powerful technique for high performance bipolar-transistor based VCO design.

A transistor-level, design-intensive overview of high speed and high frequency monolithic integrated circuits for wireless and broadband systems from 2 GHz to 200 GHz, this comprehensive text covers high-speed, RF, mm-wave, and optical fibre circuits using nanoscale CMOS, SiGe BiCMOS, and III-V technologies. Step-by-step design methodologies, end-of chapter problems, and practical simulation and design projects are provided, making this an ideal resource for senior undergraduate and graduate courses in circuit design. With an emphasis on device-circuit topology interaction and optimization, it gives circuit designers and students alike an in-depth understanding of device structures and process limitations affecting circuit performance.

Abstract: The design of voltage-controlled Oscillators nowadays is all about being capable of operating at higher clock frequencies for the purpose of higher data rate, consuming less power for the purpose of longer battery life, and having better phase noise performance for the purpose of higher quality of wireless service and more efficient use of the available frequency spectrum since most of the wireless and mobile terminals that these VCOs work in are required to be able to operate in multiple RF standards to serve new generations of standards while being backward compatible with existing ones, leading to a demand for multi-standard multi-band radio operation that deals with high frequency RF signals that undergo different modulation schemes of different standards in different channels over a wide range of frequency band. A top-down system design from the PLL to the VCO is carried out to determine the specifications for a fully integrated dual-band voltage-controlled oscillator (VCO) designed for a Zero-IF WiMAX/WLAN receiver in a O.18tm CMOS technology with 1.8V supply voltage. A VCO employing a differential cross-coupled inductance-capacitance (LC) tank architecture is proposed to cover twice the desired frequency bands for WiMAX and WLAN standards in order to avoid load pulling between VCO frequency and incoming RF frequency. The switching between two bands is implemented by using two binary-weighted capacitor arrays while switching inside each sub-band is implemented by different

digital control signal combinations for the binary-weighted capacitances. A phase noise of -120.7dB/Hz at 1MHz offset frequency is demonstrated for an oscillation frequency of 4.84GHz. The average power consumption of this VCO is 8.1mW. This VCO is developed as an IP (Intellectual Property) to be used in a fully integrated CMOS multi-standard WiMAX/WLAN radio allowing seamless roaming of handheld mobile devices between hotspots in future Wireless Metropolitan Area Network (WMAN). To compare the performance of ring oscillators to that of LC tank oscillators, the designs of two three-stage multiple-pass voltage-controlled ring oscillators with dual-delay paths are demonstrated where the differential delay cell utilizes both the primary loop delay and the negative skewed delay to increase the frequency of oscillation substantially and retain or even increase tuning range. Their phase noise performance is also improved by switching in and out the transistors periodically. In design I, the covered frequency range is from 0.74 GHz to 1.96 GHz, which translates to a tuning range of 90 % A phase noise of -104.995dBc/Hz is demonstrated for an oscillation frequency of 1.8535 GHz. Each stage draws a current of 4.963mA on average from a 1.8V power supply, resulting in a power consumption of 26.8mW. In design II, the covered frequency range is from 1.0478 GHz to 2.0022 GHz, which translates to a tuning range of 63%. The frequency-voltage curve is almost a perfect linear curve for V between OV and 0.9V. A phase noise of -110.O45dBc/Hz is demonstrated for an oscillation frequency of 2.00216 GHz. Each stage draws a current of 10.179mA on average from a 1.8V power supply, resulting in a power consumption of 55mW.